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TRANSPORT DELAY MEASUREMENTS: METHODOLOGY AND ANALYSIS FOR THE F-16C COMBAT ENGAGEMENT TRAINER, THE DISPLAY FOR ADVANCED RESEARCH AND TRAINING, AND THE F-16A LIMITED FIELD OF VIEW

Roger W. Leinenwever
Susanne I. Moran

GE Government Services, Incorporated
General Electric Company
P.O. Box 137
Gilbert, AZ 85234

HUMAN RESOURCES DIRECTORATE
AIRCREW TRAINING RESEARCH DIVISION
Williams Air Force Base, AZ 85240-6457

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Roger W. Leinenwever
Susanne I. Moran

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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General Electric Company
P.O. Box 137
Gilbert, AZ 85234

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Transport delays between the cockpit and visual/sensors in simulation systems can result in significant degradation of flight simulation training. At the Armstrong Laboratory, Aircrew Training Research Division, methodologies for testing visible delays were developed and measurements run on three systems. The tests showed significant transport delays; in some cases, higher than anticipated. Further analysis of the data revealed that the delays were caused by specific hardware and software configurations. Changes in configurations can eliminate the problem entirely, or can decrease transport delays to an acceptable range.

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PREFACE

This paper presents the methodology and analysis of transport delay measurements taken at the Armstrong Laboratory Human Resources Directorate – Aircrew Training Research Division, Williams Air Force Base, Arizona, on the Combat Engagement Trainer (CET), the Display for Advanced Research and Training (DART)/CET, and the F–16A Limited Field of View (LFOV) systems. The work was done under the terms of Work Unit No. 1123–04–01, Technical Support for Visual and Sensor Scene Generators and Display Operations and Maintenance, and contract F33615–88–C–0014 with GE Government Services, Inc. The contract monitor was Mr. Daniel H. Mudd. The task monitor for the Air Force was Dr. Elizabeth L. Martin.

TRANSPORT DELAY MEASUREMENTS: METHODOLOGY AND ANALYSIS FOR THE F-16C COMBAT ENGAGEMENT TRAINER, THE DISPLAY FOR ADVANCED RESEARCH AND TRAINING, AND THE F-16A LIMITED FIELD OF VIEW

SUMMARY

This technical paper presents the methodology and analysis of transport delay measurements taken at the Armstrong Laboratory Human Resources Directorate, Aircrew Training Research Division (AL/HRA), Williams Air Force Base, Arizona, on the Combat Engagement Trainer (CET), the Display for Advanced Research and Training (DART)/CET, and the F–16A Limited Field-of-View (LFOV) systems.

To characterize the experimental apparatus used for the visual training effectiveness program, delay measurements were taken on the three systems in March 1991. The test methodology used a special software load. This load used a switch, sampled at the same point in the field as the pitch input, to trigger a +/– 80 degree pitch value in place of the computed value. For sensor change detection and high contrast visual signals, the cathode-ray tube (CRT) attitude direction indicator (ADI) and the database were changed to a white sky and black earth. Onset responses for the simulated ADI and Advanced Visual Technology System (AVTS) visuals were recorded with a chart recorder in time measurements against the activation of the discrete switch input.

Test results show that the three systems have transport delays that were expected as well as unanticipated delays ranging from moderate to high. More than half the test samples for CET #2 were beyond worst case, less for the DART/CET and F–16A LFOV. However, while the findings are significant, further analysis of the data with a systems perspective shows that most of the delays can be eliminated entirely or decreased to an acceptable range.

INTRODUCTION

This technical paper describes methods for quantification of transport delays between the cockpit and the visuals/sensors of flight simulators, and presents the results from transport delay measurements taken at AL/HRA on the CET, the DART/CET, and the F–16A LFOV systems. While the particular application was designed for part-task trainers, it can accommodate full-mission simulators as well.

Technical Background of the Problem

Transport delays in simulation systems result from hardware and software selection and utilization. Measurement of the total delay from initial input to final output is the initial desired parameter. However, if the delay is more than anticipated, internal subsystem delays will require measurement to identify the problem location.

Latency Measurements

The simplest type of measurement for total system delay is the use of discrete inputs to cause discrete outputs. In a training system using aerodynamic input controls and instruments or a visual display as the final output, the use of discrete inputs to cause a major aerodynamic change may require limited modification of software that is intrinsic to the system being tested. Care must be taken to limit any effect the changes may have on the measurement being taken.

Transport delay measurement for a training device require a high-speed recorder stylus to monitor the input and output devices. In order to eliminate additional delays that may be caused by the recording device itself, a high-speed analog chart recorder is preferred. The chart recorder stylus will not respond to the frequency change of normal video signals on a video scan line. For a usable video signal the chart recorder can display, video must be limited to a light–and–dark configuration. A small database consisting of light (white) sky and dark (black) ground will enhance video change detection during the test sequence.

Best and worst case conditions affect all transport delay measurements and frequently the delay will be referenced as the average of the best and worst cases. In synchronous transfer and sample systems, the best–case condition will occur when the event, a change in condition, occurs immediately before the sample period, thus eliminating any additional time to the transport delay of that particular measurement. The worst–case condition will occur when the event happens immediately after the sample period, thus adding a complete computational cycle of time to the transport delay of that particular measurement. To record and identify the best to worst multiple transport delays requires measurement through numerous changes and over several seconds. A variable square wave input system can be used as the input device instead of a discrete device to create the numerous changes in a controlled manner.

TRANSPORT DELAY TEST METHODOLOGIES

System End-to-End Transport Delay Test

Single Event Test

As illustrated in Figure 1, end-to-end transport delay testing requires a high–speed chart recorder to monitor the input and output device and an optional reference clock. The input device can either be a switch or a discrete on/off control, preferably on the stick or throttle. The discrete input selected for the test requires that the input sample time occurs in the same sample cycle as the pitch inputs from the stick.

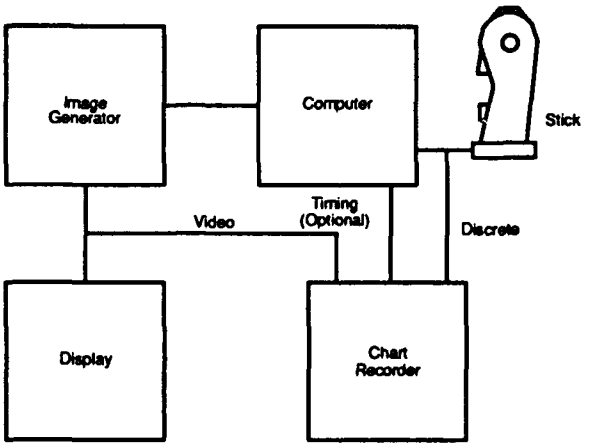


Figure 1. End–to–End Transport Delay Test

The discrete input will signal the software, to replace the pitch output from the aero equations, causing the pitch to go a predetermined +/– 80 degrees depending on the discrete position. Changes between +/– 80 degrees will occur within one computational cycle of the aero algorithms and be output to the cockpit or visual system for display. The video or instrument signal of the output device will be

monitored to observe changes in the state. The clock can be a local reference for the chart recorder or can be developed from a timing signal generated for the system in test.

The timing signal for a simulator/trainer using an image generator (IG) can be the odd/even field in a high/low format representing that field. Any offset in timing from the start of the computational cycle to the odd/even signal has to be known. Data gathered from the test require comparison with a timing diagram based on theoretical values of known or assumed operating speeds, software modules, and functions of the system under test.

Multiple Event Test

For sequential multiple event measurements, a square wave generator with a voltage output equal to the discrete device output can be used for a highly accurate frequency of change. The square wave generator requires a 50% duty cycle and a frequency setting equal to one half or less of the computational or sample cycle of the system being tested. Several seconds of data will generally produce 15 to 60 samples for latency analysis.

System Segment Transport Delay Test

Single/Multiple Event Test

A single/multiple event test is a subset of the end-to-end test and is done in the same manner as the end-to-end test with the addition of a segment response input to the chart recorder. Figure 2 illustrates that configuration.

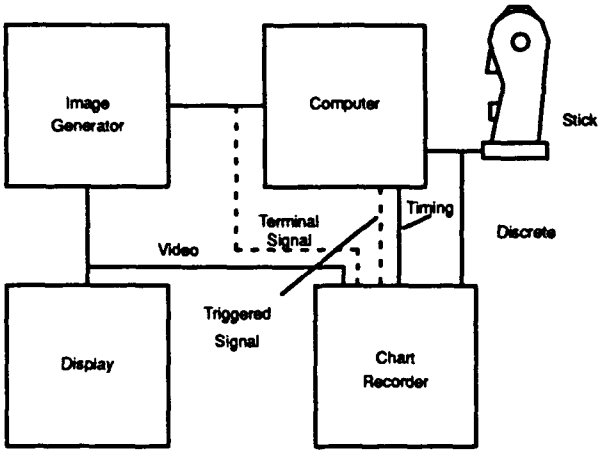


Figure 2. System Segment Transport Delay Test

A segment response may consist of the following:

1. Existing signals used in transfer functions.
2. Utilization of a hardware signal to create a triggered condition as a response.
3. A triggered condition created from a software read or write of a specific memory location.
4. A triggered condition created from an interrupt.

Delay Errors

If recognizable delay errors are detected, specific test sequences will have to be generated to further isolate the problem. Generally, simulator visual systems will respond two to three computational cycle times later than cockpit instrumentation.

Latency Data Analysis

Once the measurements have been taken and the test data generated, the tabulated data can be evaluated and plotted.

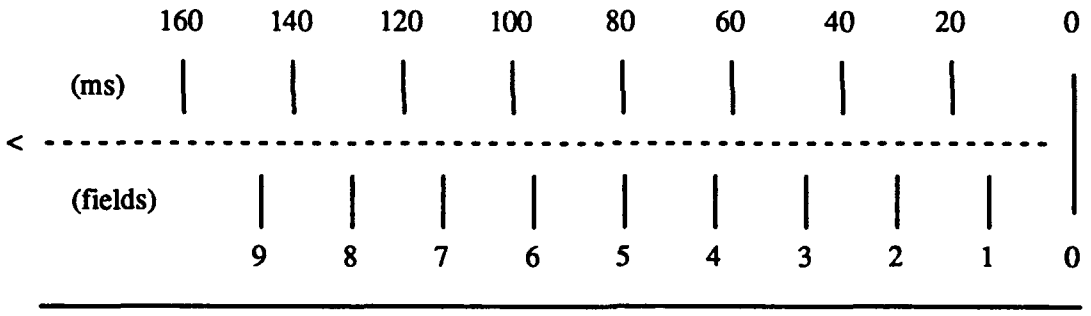
Tabulated Test Data

The tabulated test data may be evaluated with the following procedures:

1. Confirm that the first detectable visual change is evenly divided between odd and even fields.
2. Calculate the paper scale in fields per millimeter (mm) and convert the tabulated data from fields + mm to fields.
3. Summarize the range of values of time intervals in fields. At 60 Hz, convert to seconds using 16.66 milliseconds (ms) per field. For other update rates, convert equivalent ms.
4. Plot the ranges for each parameter with the following table:

Table 1. Range Plotter

Time Prior to End of First Changed Visual Field



Plotted Data

After the data are plotted, they are analyzed for statistical variance and to determine hardware conformity. The hardware conformity analysis is accomplished with the following steps:

1. Confirm that the first detectable change in the parameter being monitored occurs in conjunction with a field change for the visual or computer cycle change, based on algorithm placement within the cycle.
2. Confirm that the measurement between the first detectable change in the input, and the first detectable change in the parameter value being monitored, are always measured from the same reference. Visual signal references are measured to the beginning of the field. Sensor signals are measured to the peak of signal detection and time compensated for the offset created by physical placement of the sensor within the field of scan.
3. Confirm that the difference between the minimum/maximum values of measured parameters does not exceed the established criteria for acquisition of state changes within the system.

Event Times

On the transport delay plot for each test, the event times in fields are measured back from the end of the display field that changed, odd and even. The event times include:

1. Control input threshold; and
2. Parameter monitored change onset.

Validation of System Architecture

The transport delay plots are used for validation of the system architecture with the following procedures:

1. Verification that the monitored input and the corresponding software algorithm output always occur in the same desired frame of reference (field, frame or cycle).
2. Evaluation of all delays for consistency with known system architecture.
3. Evaluation of all relationships between measured events and the visual changes for consistency with known system architecture.

TRANSPORT DELAY TESTING

Test Preparations

Test preparations for all three systems consisted of creating a demonstration load from baselined software incorporating required changes for the testing. A switch input, sensed during the same sample period as the pitch input, was chosen for each system. The UHF switch was used on both CETs and the IFF switch was used on the F–16A. The switch triggered the software to output a pitch value of +/– 80 degrees in place of the computed pitch. For CET #2 and the DART/CET, the color of the ADI was changed to a white sky and black earth for photo sensor change detection; for the DART/CET and F–16A LFOV, the out-the-window (OTW) database was changed to a white sky and black earth, providing a high contrast visual signal.

Test Procedures

For CET #2, the UHF switch output was provided to a chart recorder as well as a signal from a photo sensitive transistor circuit attached to the CRT, over the simulated ADI, to monitor the white–and–black video. With the chart recorder operating at 200 mm per second, the UHF switch was manipulated numerous times and the data recorded. Figure 3 shows the test configuration for the CET.

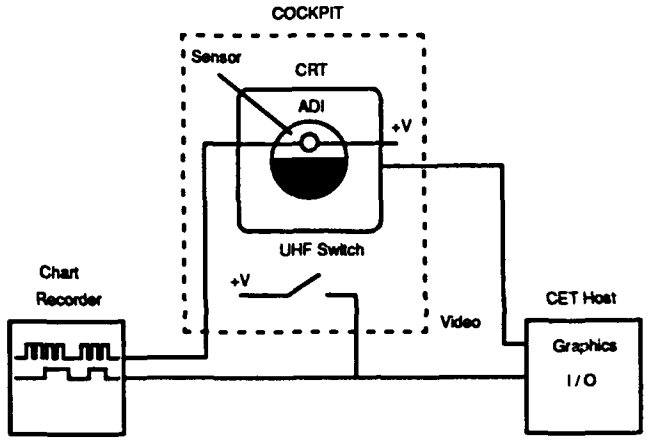


Figure 3. CET #2 Test Configuration

Test procedures for the DART/CET were the same as CET #2 with the addition of an AVTS Odd/Even field flag and the front window green video signal applied to the chart recorder. The DART/CET was tested in update rates of 60 and 30 Hz. Figure 4 shows that configuration.

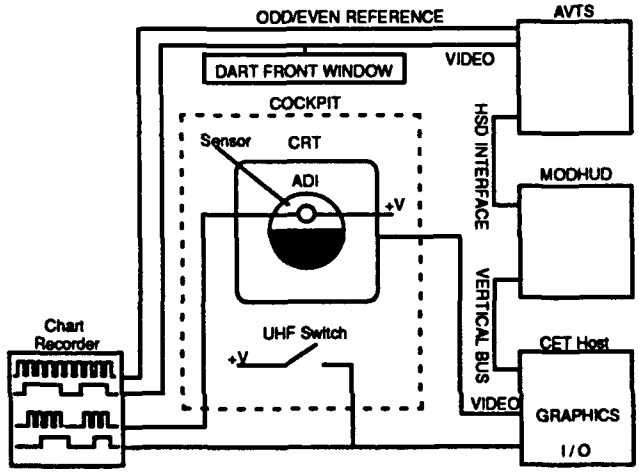


Figure 4. DART/CET Test Configuration

The F–16A testing followed the CET and DART/CET procedures with the exception of using the IFF Idcnt switch to toggle the ADI and video scene. In place of the ADI photo sensor input to the chart recorder, the analog ADI X signal value was used along with the background green video. To properly account for possible differences in aero computations affecting the transport delay measurements, testing was done in both freeze and flight modes. The measurements were taken at 10 samples per sample period.

The F–16A was also tested separately with the headtracker operating and not operating. Figure 5 illustrates the test configuration. The measurements taken used 20 samples per sample period (run) and two runs per configuration. The expanded view of the system showed that the average of best and worst cases for the four runs, two with and two without the headtracker, were closely aligned with each other and within the measurement accuracies expected. The data suggest that use of the headtracker has no noticeable effect on visual responses.

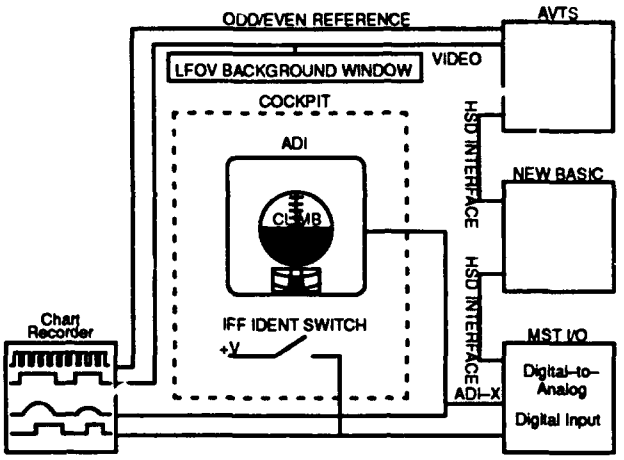


Figure 5. F-16A LFOV Test Configuration

TRANSPORT DELAY ANALYSIS

CET #2

Based on the 30 Hz central processing unit (CPU) cycles, software module positioning, and a 15 Hz update rate of the double buffered graphics output module, the best case response for the ADI was approximately 140 ms after switch, or stick, initiation. The CPUs in CET #2 are not synchronized, and the best-and worst-case conditions will always change within some parameters based on the clock oscillator in each CPU. Figure 6 represents the anticipated time line flow for CET #2 without consideration for the variation of CPU oscillators. Table 2 summarizes the chart recorder data.

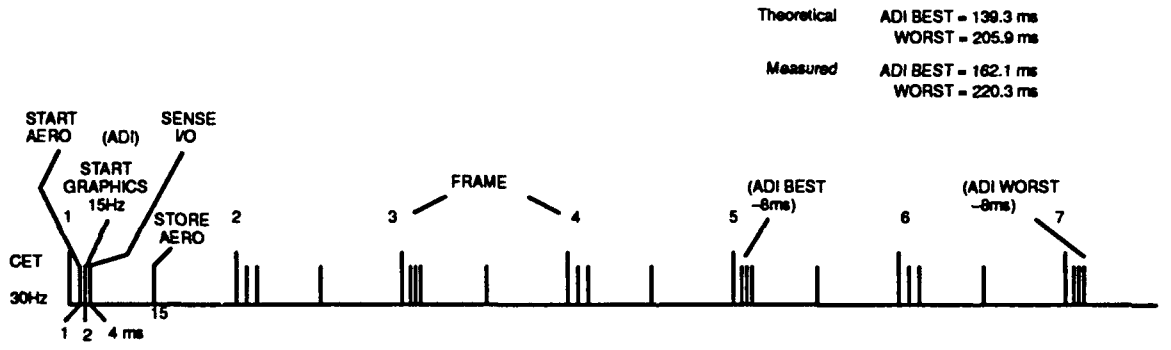


Figure 6. CET 30 Hz Timing

Minimum and maximum variations were slightly less than two 30 Hz cycles, which is anticipated since the ADI is updated at 15 Hz and the input/output (I/O) was sampled at 30 Hz. However, the average delay for the ADI, based on minimum and maximum values, was nearly equal to worst-case timing: 62% of the samples were equal to or greater than worst-case timing.

Table 2. CET Transport Delays

A	B	C
Sample #	mm Readings	ms ADI
1	41.75	206.68
2	44.50	220.30
3	41.50	205.45
4	43.25	214.11
5	38.25	189.36
6	38.25	189.36
7	32.75	162.13
8	44.75	221.53

A = Number of samples
B = Reading in millimeters between switch activation and ADI response.
C = Reading in milliseconds of ADI response.

Mean of sampled ADI Values (ms)	Min/Max Variation of ADI (ms)	Average # of 30 Hz Frame	Average ms for ADI (Min+Max) /2 (ms)
201.11	59.41	5.75	191.83

Samples greater than worst case may be due to the lack of synchronization between the CPUs or to cycle overruns on a particular CPU. Table 3 summarizes theoretical, measured, and optimized goals with best/worst case values for each system.

Table 3. Transport Delay Summary

	Theoretical (ms)	Measured (ms)	Optimized (ms)
CET			
ADI Best	139.9	162.1	100.0
Worst	205.9	220.3	133.3
DART 30			
ADI Best	139.3	158.9	100.0
Worst	205.9	228.9	133.3
Vis Best	165.5	233.1	133.3
Worst	198.8	266.1	166.6
DART 60			
ADI Best	139.3	155.9	100.0
Worst	205.9	222.7	133.3
Vis Best	115.4	183.6	83.3
Worst	148.7	211.6	116.6
F-16A LFOV			
ADI Best	20.0	61.8	20.0
Worst	36.6	76.7	36.6
Vis Best	68.0	97.7	67.7
Worst	84.6	127.5	84.3

Theoretical = Transport delay based on present hardware and software design and alignment.
Measured = Transport delay measured
Optimized = Transport delay based on present hardware and properly aligned software

DART/CET

The DART/CET and the modular head-up display (MODHUD) chassis are interlinked by a high speedbus system which makes each chassis an extension of the other. The DART/CET CPUs are synchronized to some degree with the high speed data (HSD) transfer between the AVTS and the MODHUD. However, the DART/CET has the same software module placement as CET #2 with the same corresponding results for the ADI.

The DART/CET was tested with the AVTS visual at 60 and 30 Hz update rates. Figure 7 shows the anticipated time flow at 60 Hz. Table 4 summarizes the chart recorder data for 60 and 30 Hz testing. Again, the DART/CET shows two 30 Hz cycles, anticipated because of the 15 Hz update of the graphics. However, the average delay for the ADI was almost one half cycle: 16 ms greater than anticipated with 18% of the samples beyond the worst case.

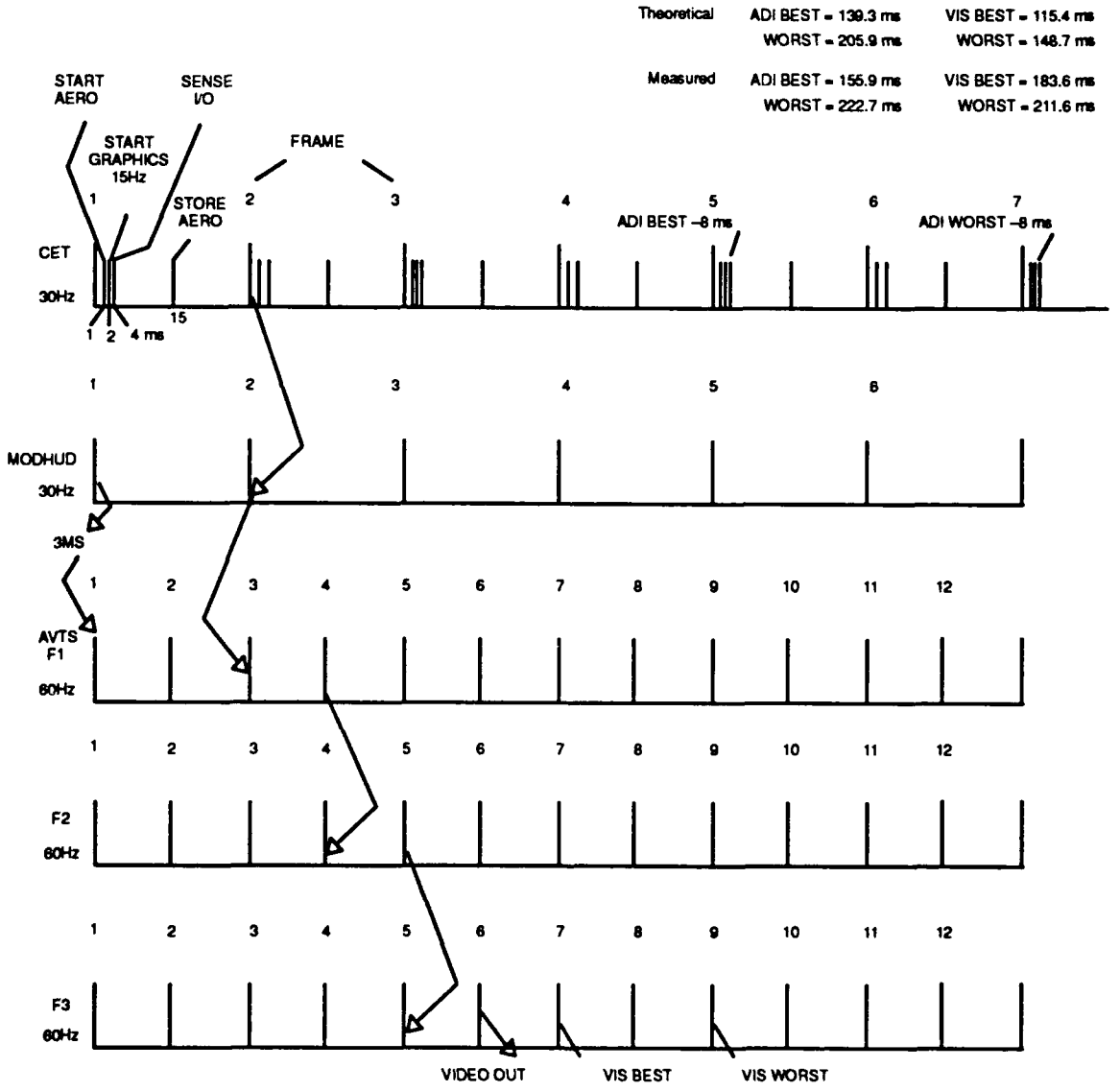


Figure 7. DART/CET Anticipated Time Flow at 60 Hz

Table 4. DART/CET Transport Delays

[60 Hz]				[30 Hz]		
A	B	C	D	E	F	G
Sample #	mm = .5 Readings	ADI ms	Vis ms	mm = .5 Readings	ADI ms	Vis ms
1	37.0	183.17		38.4	189.85	
	37.5		185.64	47.4		234.41
2	33.3	164.60		36.6	181.19	
	40.0		198.02	51.4		254.21
3	39.8	196.78		43.5	215.35	
	39.3		194.31	51.6		255.45
4	31.5	155.94		43.3	214.11	
	37.5		185.64	50.8		251.24
5	33.5	165.84		38.3	189.36	
	39.4		194.80	52.7		260.64
6	42.8	211.63		43.3	219.06	
	41.0		202.97	51.3		253.71
7	35.9	177.48		46.3	228.96	
	41.0		202.97	53.8		266.09
8	37.8	186.88		40.5	200.50	
	42.6		210.89	47.5		235.15
9	35.3	174.50		40.1	198.51	
	40.3		199.26	50.5		250.00
10	33.0	163.37		42.5	210.40	
	37.1		183.66	52.3		258.91
11	45.0	222.77		32.1	158.91	
	42.8		211.63	48.1		238.12
12				38.0	188.12	
				47.1		233.17
13				34.5	170.79	
				50.5		250.00
14				33.3	164.60	
				48.5		240.10

A = Number of samples
B, E = Reading in millimeters between switch activation and response.
C, F = Reading in milliseconds of ADI response
D, G = Reading in milliseconds of visual response

Table 4. Concluded

60 Hz			
Sample Mean ADI (ms)	Min/Max Var ADI (ms)	Min/Max Var Vis (ms)	Sample Mean Vis (ms)
182.09	66.83	27.97	197.25

Average # of 30 Hz Frames	Average ms for ADI (Min+Max) /2	Average ms for Vis (Min+Max) /2	Average # of 60 Hz Frames
5.68	189.36	197.65	11.86

30 Hz			
Sample Mean ADI	Min/Max Var ADI (ms)	Min/Max Var Vis (ms)	Sample Mean Vis (ms)
194.98	70.05	32.92	248.66

Average # of 30 Hz Frames	Average ms for ADI (Min+Max) /2	Average ms for Vis (Min+Max) /2	Average # of 60 Hz Frames
5.82	193.94	249.63	7.49

At the 30 Hz update rate and with AVTS synchronized, there may have been an effect on the CPU synchronization. No change in the ADI readings was expected. However, the minimum and maximum average delays for the ADI increased by approximately four to five ms. This may indicate a need to confirm the AVTS timing scheme between 60 and 30 Hz. Figure 8 shows the anticipated time flow for the 30 Hz.

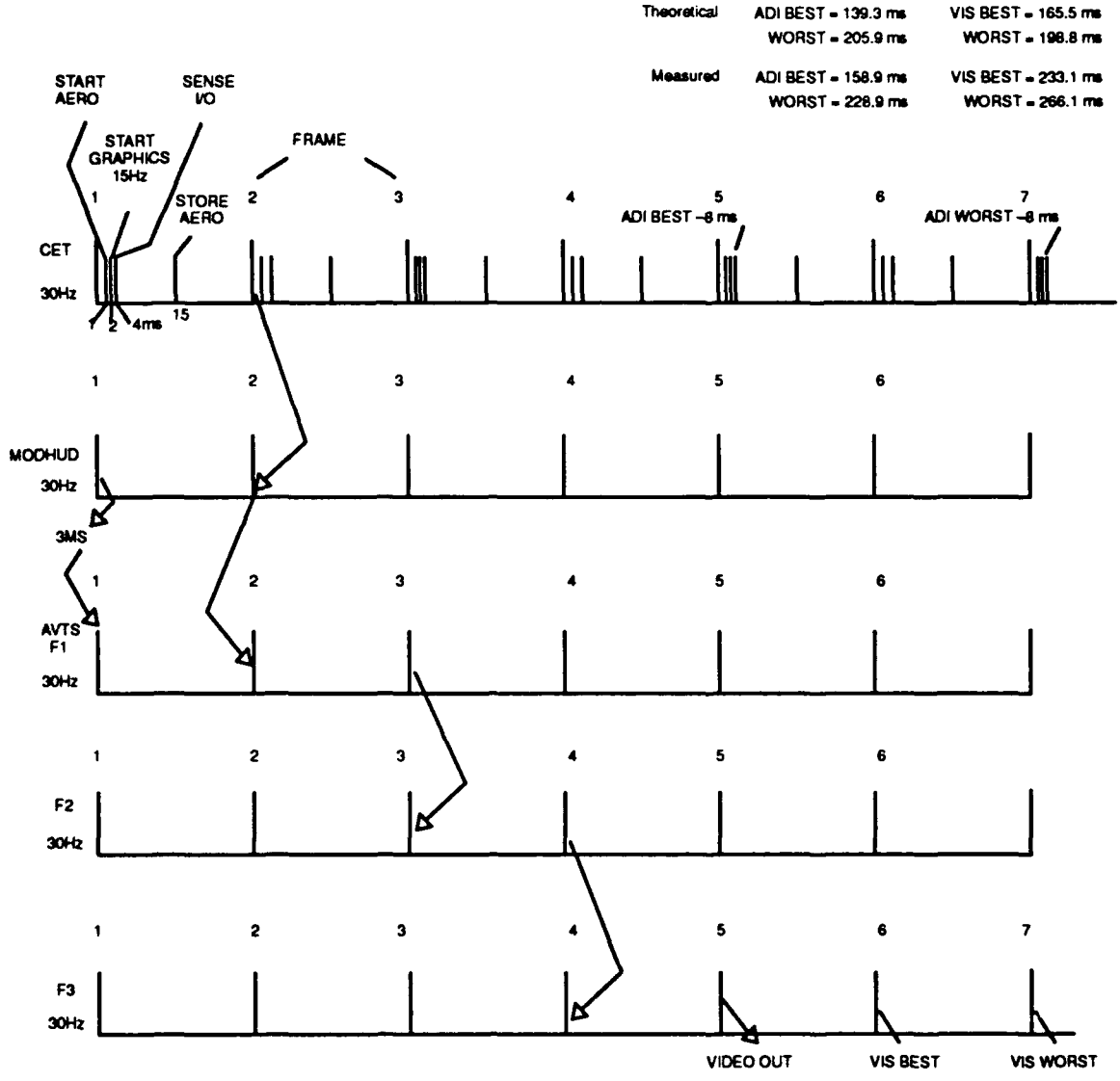


Figure 8. DART/CET Anticipated Time Flow at 30 Hz

Testing of the AVTS visuals at 60 and 30 Hz showed minimum and maximum responses within one 30 Hz cycle, which was anticipated based on switch activation time and sample speed. However, the average delay was considerably higher than expected: at least two 30 Hz Versa Modula Europa (VME) CPU cycles greater than anticipated. The maximum variation was approximately 63 ms greater than the expected worst case at 60 Hz and 67 ms at 30 Hz, which represents almost two 30 Hz CPU cycle times of additional delay. The AVTS does have a 60 Hz field synchronization implementation that requires some software manipulation to communicate at 30 Hz, not considered at the time of data gathering. That may explain one 30 Hz cycle delay.

F-16A LFOV

The F-16A cockpit is connected to the Microprocessor Simulation System (MST) VME-based I/O, which is interfaced to the basic computer system via an HSD. The 60 Hz MST HSD transfer is synchronized to the basic computer system, which is, in turn, synchronized to the AVTS visual computer system. Testing was done in ADI and visual flight and freeze modes with minimum delays expected. Figures 9 and 10 show the anticipated time flow; Table 5 summarizes the chart recorder data.

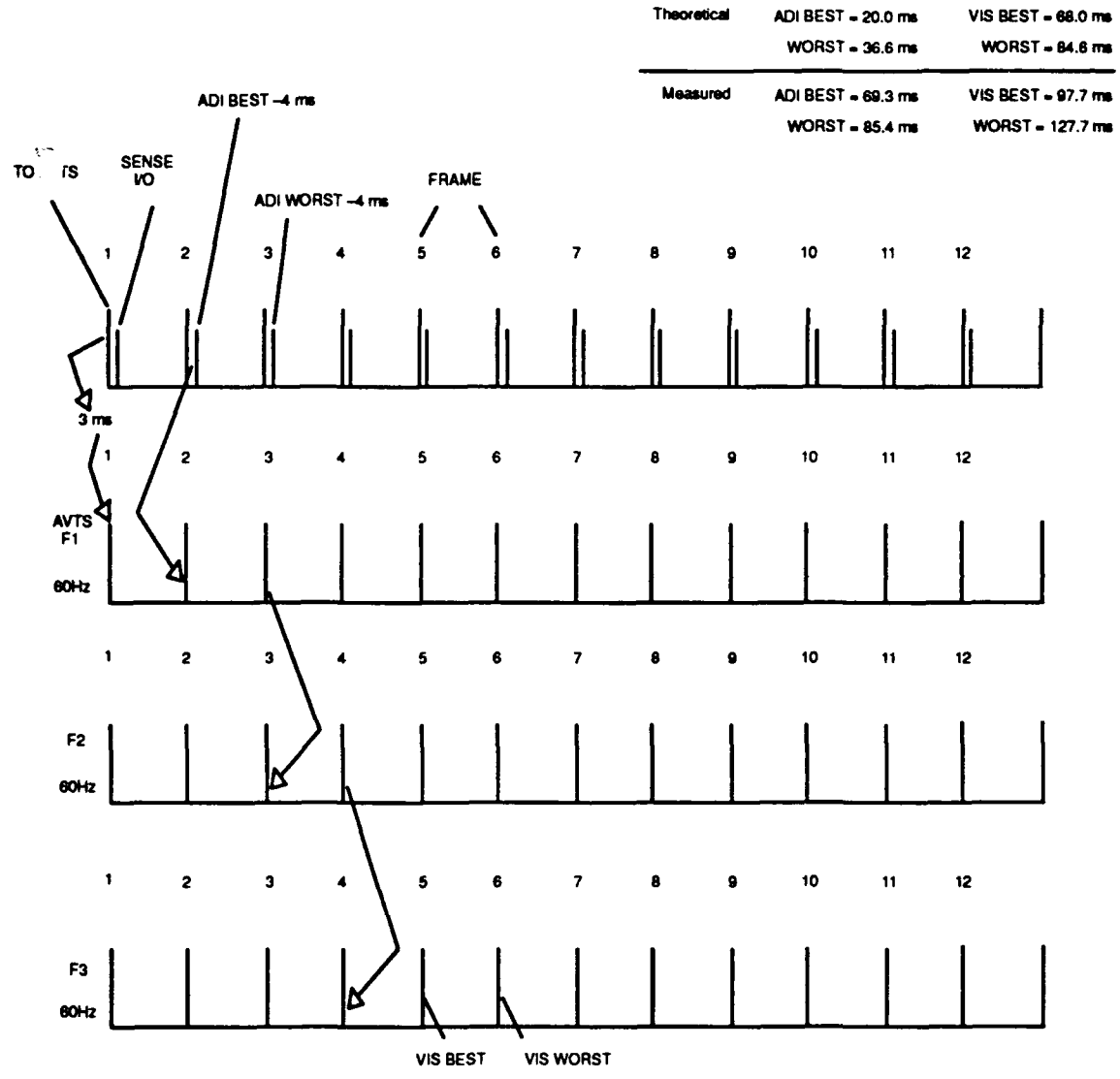


Figure 9. F-16A 60 Hz Timing - Freeze Mode

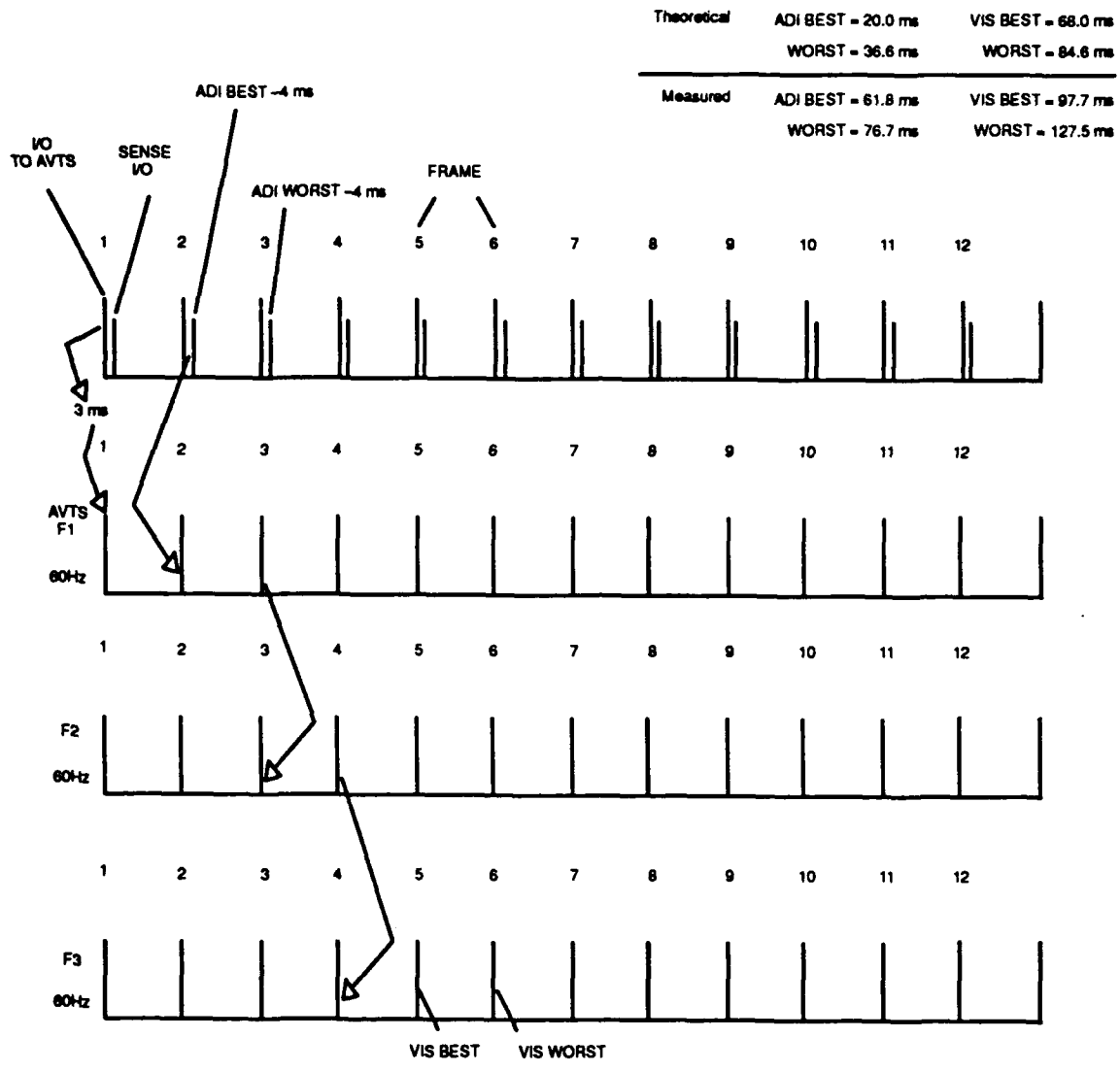


Figure 10. F–16A 60 Hz Timing – Flight Mode

Table 5. F–16A Transport Delays

	Freeze Mode			Flight Mode		
A	B	C	D	E	F	G
Sample #	mm = .5 Readings	ADI ms	Vis ms	mm = .5 Readings	ADI ms	Vis ms
1	14.3	70.79		12.5	61.88	
	23.6		116.83	19.8		97.77
2	15.1	75.50		15.0	74.26	
	21.3		105.20	21.9		108.17
3	14.5	71.78		14.1	69.80	
	21.5		106.44	25.8		127.48
4	17.3	85.40		15.5	76.73	
	19.8		97.77	21.0		103.96
5	14.5	71.78		14.1	69.80	
	20.8		102.72	21.5		106.44
6	16.5	81.68		14.6	72.28	
	25.8		127.48	21.3		105.20
7	15.3	75.50		13.0	64.36	
	25.8		127.72	24.4		120.54
8	14.0	69.31		14.7	72.77	
	25.5		126.24	20.0		99.01
9	15.0	74.26		14.1	69.80	
	24.1		119.31	21.0		106.44
10	15.3	75.74		13.5	66.83	
	21.5		106.44	20.0		99.01

A = Number of samples
B, E = Reading in millimeters between switch activation and response.
C, F = Reading in milliseconds of ADI response
D, G = Reading in milliseconds of visual response

Table 5. F–16A Concluded

Freeze Mode			
Sample Mean ADI (ms)	Min/Max Var ADI (ms)	Min/Max Var Vis (ms)	Sample Mean Vis (ms)
75.17	16.09	29.95	113.61

Average # of 30 Hz Frames	Average ms for ADI (Min+Max) /2	Average ms for Vis (Min+Max) /2	Average # of 60 Hz Frames
4.64	77.35	112.75	6.76

Flight Mode			
Sample Mean ADI (ms)	Min/Max Var ADI (ms)	Min/Max Var Vis (ms)	Sample Mean Vis (ms)
69.85	14.85	29.70	107.40

Average # of 30 Hz Frames	Average ms for ADI (Min+Max) /2	Average ms for Vis (Min+Max) /2	Average # of 60 Hz Frames
4.16	69.31	112.62	6.76

The minimum and maximum variation for the ADI was within expected parameters based on the activation of the switch and the I/O sample speed. The problem was an additional 40 ms delay in both the best and worst case based on predicted values. The only explanation for a delay of that magnitude is that some portion of the ADI computation was running at 30 Hz along with the possibility that the MST may not be outputting the I/O data within a four ms window after transmission from the host.

The ADI freeze mode testing showed an additional 10 ms gained, causing a 50 ms difference on both the best and worst case measurements from the predicted values. While that should not present a problem because the system is not operated in that configuration, the delays could indicate possible overrun conditions on the basic computer system.

Testing in visual flight and freeze modes showed almost identical results. The best case condition for the F–16A should be about one ms over four 60 Hz frame times. However, the minimum and maximum variations were approximately two 60 Hz frames, which indicates either the aero computations or the MST I/O functions are not operating effectively at 60 Hz. There was also a difference of more than two 60 Hz frames beyond the worst case, which would indicate that another frame and a half of delays were occurring over and above the frame being induced. This was almost identical to the problem seen with the ADI, and a strong probability exists that the delays are caused by software either being out of sequence or operating at 30 Hz.

Data from the tests of the F–16A with the headtracker, did, however, shed some light on the measurements taken on that system without the headtracker. Minimum and maximum variation for the ADI in the F–16A cockpit with the headtracker was beyond expected parameters based on the activation of the switch and the 60 Hz I/O sample speed. The data show up to one 30 Hz cycle time of difference between minimum and maximum readings. That difference may explain the unexpectedly high delay found earlier for the F–16A. As suspected, it is most likely that when the earlier delays were measured, some portion of the I/O sensing and/or ADI/visual computations were not running effectively at 60 Hz.

RECOMMENDATIONS

It should be noted that the software under test for CET #2, the DART/CET, and the F–16A instrumentation has never been optimized to minimize transport delay. Hence, while the delays were occasionally high, present software arrangements may account for most of the latency.

CET #2

For CET #2, improvements in the ADI response times can be accomplished with synchronization of the CPUs and proper arrangement of the software modules within each CPU. If a 15 Hz update rate is the maximum the graphics module can accommodate, 100 to 133 ms response will be the best/worst cases.

DART/CET

For the DART/CET, improvements in the ADI response times can be made with proper arrangement of the software modules within each CPU. CPU synchronization should be done first to eliminate nonsynchronization as the only transport delay problem. If a 15 Hz update rate is the maximum the graphics module can accommodate, 100 to 133 ms response will be the best/worst case.

Some improvements in the visual response, for both the 30 and 60 Hz versions, will be a natural fallout of restructuring the CET software. An additional improvement could come if the AVTS field synchronization was incorrect at the time of the test, for 30 Hz, and a failproof method is incorporated for 30 Hz synchronization.

F–16A LFOV

It is most likely that improvements in the ADI response times can also be made for the F–16A with proper arrangement of the software modules in the basic computer system. Improvements in the visual response should follow with software restructuring. If that is not the case, additional tests are required to further isolate the problem. Timing tests between the AVTS master timing system and HSD transfer cycles for the MST/basic computer and basic computer/AVTS Frame 1 computer should confirm proper 60 Hz sequenced operations.

LIST OF ABBREVIATIONS

ADI	—	Attitude Direction Indicator
AL/HRA	—	Armstrong Laboratory Human Resources Directorate, Aircrew Training Research Division
AVTS	—	Advanced Visual Technology System
CET	—	Combat Engagement Trainer
CPU	—	Central Processing Unit
CRT	—	Cathode Ray Tube
DART	—	Display for Advanced Research and Training
GEGS	—	GE Government Services, Inc.
HSD	—	High Speed Data
IFF	—	Identification Friend/Foe
IG	—	Image Generator
I/O	—	Input/Output
LFOV	—	Limited Field-of-View
mm	—	Millimeters
MODHUD	—	Modular Head–up Display
ms	—	Milliseconds
MST	—	Microprocessor Simulation System
UHF	—	Ultra High Frequency
VME	—	Versa Module Europa

GLOSSARY

Aero Algorithms	The aerodynamic algorithms required to represent the movements of the aircraft on the visuals/sensors
Chart Recorder	A high speed device used to measure transport delays
Computational Cycle	The time to complete processing for a single frame
Database	Computer-generated terrain
Hz Rate	The number of times a visual display is updated (refreshed) in a second
Image Generator	A computer generating visual displays
Modular HUD	A head-up display in the cockpit that is generated separately from the visual display, and is projected over the terrain
Multiple Event Test	Collection of data on several repeated events
Part-Task Trainer	A training simulator that trains specific tasks
Pitch Value	An angle of aircraft pitch in degrees
Single Event Test	Testing and data gathering on a discrete event
Statistical Variance	The square of the standard deviation
Synchronous Transfer	Clocked transfer of data between the cockpit and visuals/sensors
System Architecture	The building blocks of systems hardware and software
Transport Delay	The time delay between cockpit controls and movements on visuals/sensors in simulators